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09/807,625	04/16/2001	Isao Isogai	L9289.01130	2014

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EXAMINER	
SHRADER, LAWRENCE J	
ART UNIT	**PAPER NUMBER**
2124	4

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/807,625	ISOGAI, ISAO	
	Examiner	Art Unit	
	Lawrence Shrader	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The claim is structured as a preamble with no body. It is written as a function without any steps, being indefinite in that it fails to point out what is included or excluded by the claim. Also the claim wording is redundant causing the claim to be unclear.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Hayashi et al., U.S. Patent 6,341,239 (hereinafter referred to as Hayashi).

Hayashi discloses a program rewrite method

In regard to claim 1:

> *"A software rewriting method that detects unexecuted parts of software to be rewritten during execution of the software to be rewritten and rewrites the unexecuted parts sequentially."*

Hayashi discloses a software rewriting method that detects abnormal (unexecuted) software in memory by detecting an execution status, and rewrites the code from an external unit (column 2, lines 49 – 53) in a sequential manner via a loop (column 7, lines 50 – 53).

In regard to claim 2, incorporating the rejection of claim 1:

> *"...wherein the software to be rewritten is software having one block or software, which is divided into a plurality of blocks, and the respective blocks are classified into executing blocks and unexecuted blocks, and the unexecuted blocks are sequentially rewritten."*

Hayashi discloses the software program is written into an erased block (column 7, lines 1 – 9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al., U.S. Patent 6,341,239 in view of Ravichandran, U.S. Patent 5,966,536.

In regard to claim 3, incorporating the rejection of claim 2:

> *"...wherein rewriting blocks are temporarily stored in a memory, the rewriting blocks are compared with the executing blocks, and when blocks corresponding to the rewriting blocks are unexecuted, the corresponding blocks of the software to be rewritten are sequentially rewritten to the rewriting blocks."*

Hayashi discloses a software rewriting method that detects abnormal (unexecuted) software in memory by detecting an execution status, and rewrites the code from an external unit (column 2, lines 49 – 53) in a sequential manner via a loop (column 7, lines 50 – 53) into an erased block (column 7, lines 1 – 9), but does not explicitly disclose that the rewriting blocks are compared with the executing blocks before rewriting. However, Ravichandran discloses the comparison of blocks of executable code. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the rewrite blocks of executable code from an external source as taught by Hayashi with the comparison of blocks of executable code as taught by Ravichandran, because the combination produces a the ability to compare the rewrite code with metrics that determine whether or not the code is similarly optimized without rewriting the optimizer as taught by Ravichandran at column 2, lines 31 – 36.

In regard to claim 4, incorporating the rejection of 3:

> *"...wherein it is determined as to whether or not the corresponding blocks of the software to be rewritten are finished rewriting, and no rewriting of the corresponding blocks, which have been rewritten, are carried out again."*

See Figure 4 of Hayashi.

In regard to claim 5:

A software rewriting apparatus comprising:

"a software storage for storing software having one block or a plurality of divided blocks;"

Hayashi discloses the software program is written from a storage unit into an erased block (column 7, lines 1 – 9).

"a processor for expanding the blocks to be executed;"

See Figure 1 and related text of Hayashi.

"a block storage for temporarily storing rewriting blocks;"

See Figure 1 (rewrite unit) and related text of Hayashi.

"a discriminator for comparing the rewriting blocks with blocks executed by the processor to discriminate execution states of the blocks corresponding to the rewriting blocks; and
a rewriter for performing rewrite processing in which the corresponding blocks stored in the software storage are sequentially rewritten to the rewriting blocks in accordance with a discrimination result."

Hayashi discloses a software rewriting method that detects abnormal (unexecuted) software in memory by detecting an execution status, and rewrites the code from an external unit (column 2, lines 49 – 53) in a sequential manner via a loop (column 7, lines 50 – 53) into an erased block (column 7, lines 1 – 9), but does not explicitly disclose that the rewriting blocks are compared with the executing blocks before rewriting. However, Ravichandran discloses the comparison of blocks of executable code. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the rewrite blocks of executable code from an external source as taught by Hayashi with the comparison of blocks of executable code as taught by Ravichandran, because the combination produces a the ability to compare the

rewrite code with metrics that determine whether or not the code is similarly optimized without rewriting the optimizer as taught by Ravichandran at column 2, lines 31 – 36.

In regard to claim 10 (an terminal apparatus), it is rejected for the same corresponding reasons put forth in the rejection of claim 5 (a corresponding software writing apparatus)

6. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al., U.S. Patent 6,341,239 in view of Ravichandran, U.S. Patent 5,966,536, and further in view of Tanaka et al., JP 08085044 (hereinafter referred to as Tanaka).

In regard to claim 6, incorporating the rejection of claim 5:

> *"...wherein the discriminator comprises a table including configuration items having an item indicative of block numbers of the rewriting blocks and an item indicative of execution states of the blocks corresponding to the rewriting blocks, and the rewriter performs rewrite processing with reference to the table."*

Hayashi discloses a software rewriting method that detects abnormal (unexecuted) software in memory by detecting execution states, and rewrites the code from an external unit (column 2, lines 49 – 53) in a sequential manner via a loop (column 7, lines 50 – 53) into an erased block (column 7, lines 1 – 9), and Ravichandran discloses optimization metrics (configuration items) to compare execution blocks (column 2, lines 51 – 56), but neither Hayashi nor Ravichandran discloses a table including the configuration items including block numbers. However, Tanaka discloses an execution state table including block numbers. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the rewrite blocks of executable code from an external source as taught by Hayashi with the

comparison of blocks of executable code as taught by Ravichandran, and further combine the execution state table of Tanaka that also stores block number because the combination produces a the ability to compare the rewrite code with metrics that determine whether or not the code is similarly optimized without rewriting the optimizer as taught by Ravichandran at column 2, lines 31 – 36 and also to track the proper block numbers in a table with a corresponding execution state as taught by Tanaka.

In regard to claim 7, incorporating the rejection of claim 6:

> *"...wherein the table including a configuration item having an item indicative of rewriting states of the blocks corresponding to the rewriting blocks."*

Hayashi discloses a monitor of the execution state of the software program (column 2, lines 49 – 53).

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al., U.S. Patent 6,341,239 in view of Ravichandran, U.S. Patent 5,966,536, and further in view of Kawahara, U.S. Patent 6,393,393.

In regard to claim 8, incorporating the rejection of claim 5:

> *"...further comprising a controller for surveying a degree of load of processing executed by a CPU, and instructing the rewriter to carry out rewrite processing when the degree of load becomes low."*

In regard to claim 9, incorporating the rejection of claim 8:

> *"...wherein the controller surveys the degree of load of processing executed by the CPU in response to a rewrite request sent from the rewriter."*

Hayashi discloses a software rewriting method that detects abnormal (unexecuted) software in memory by detecting execution states, and rewrites the code from an external unit

(column 2, lines 49 – 53) in a sequential manner via a loop (column 7, lines 50 – 53) into an erased block (column 7, lines 1 – 9), and Ravichandran discloses optimization metrics (configuration items) to compare execution blocks (column 2, lines 51 – 56), but neither Hayashi nor Ravichandran discloses a CPU load monitor wherein a signal is given to perform a rewrite based on the CPU load. However, Kawahara discloses a CPU load monitor with the ability to signal a specific action based on the CPU load threshold (column 8, lines 43 – 49; e.g., Figure 2). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the rewrite blocks of executable code from an external source as taught by Hayashi with the comparison of blocks of executable code as taught by Ravichandran, and further combine the CPU load monitor and threshold signal of Kawahara because the combination produces a the ability to compare the rewrite code with metrics that determine whether or not the CPU is loaded at a certain threshold an signal the rewriter according to the optimization metrics as taught by Ravichandran.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046. The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence Shrader
Examiner
Art Unit 2124

26 April 2004

TODD INGBERG
PRIMARY EXAMINER